Best Available Copy



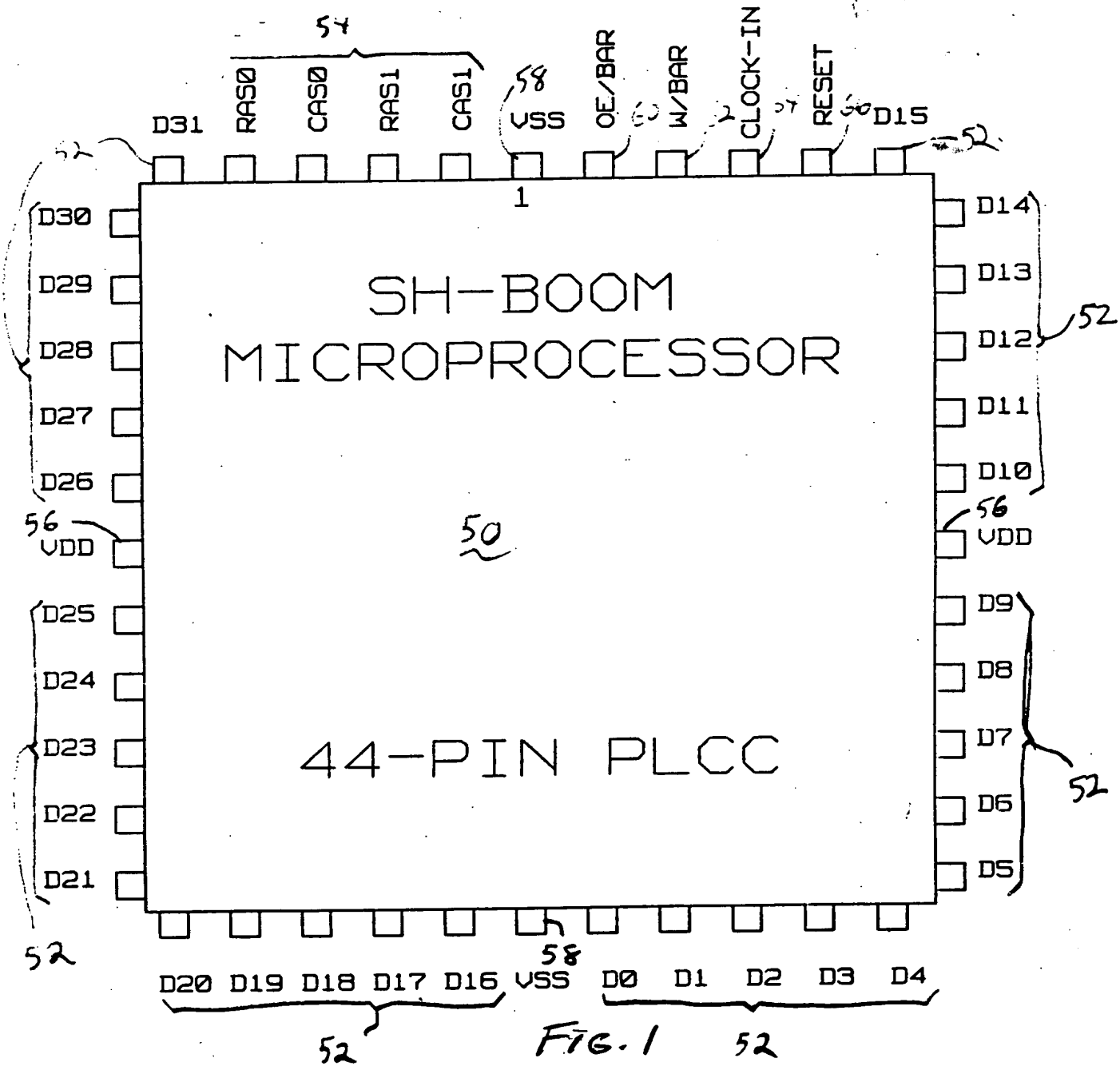


FIG. 1

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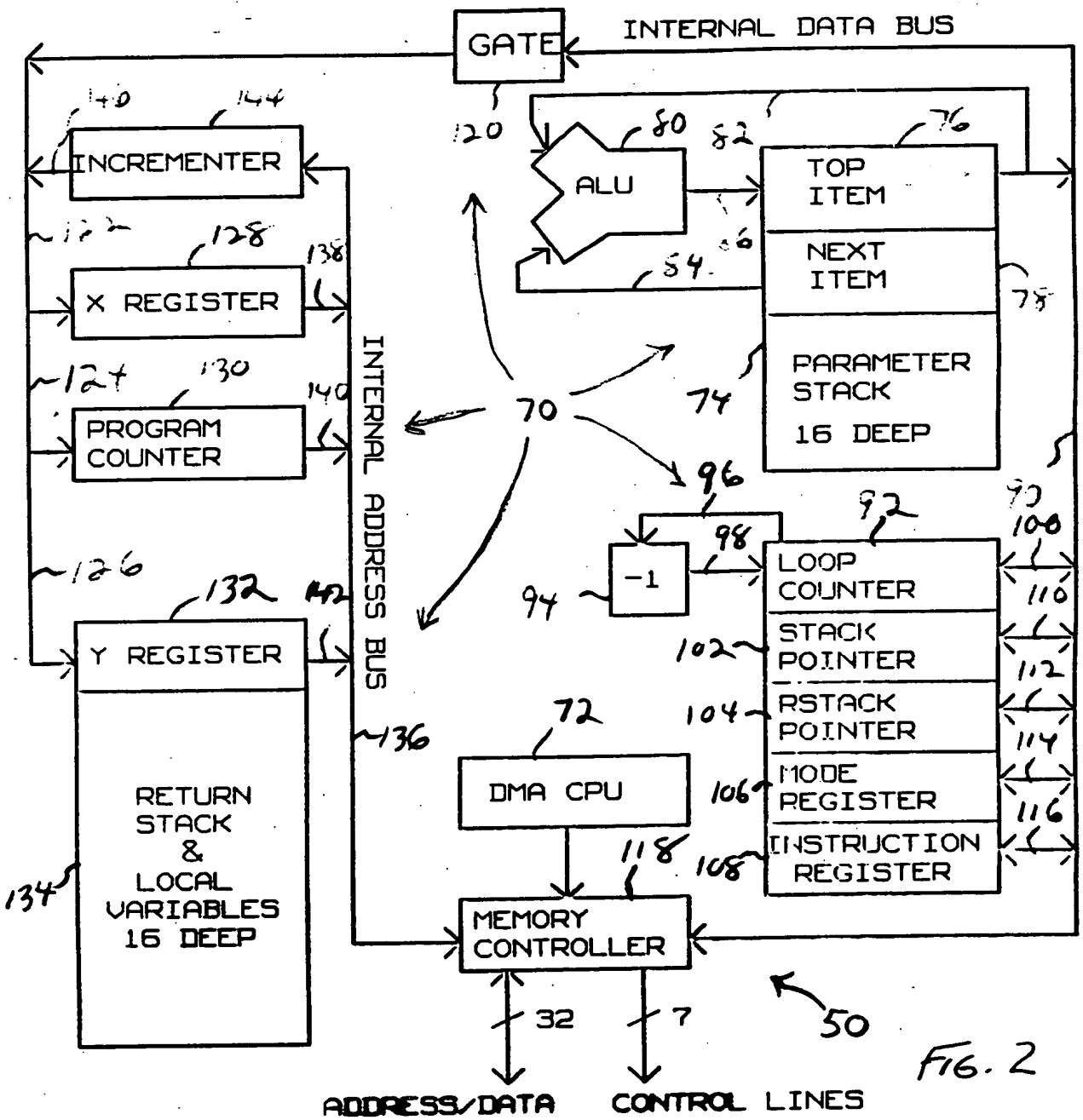


FIG. 2

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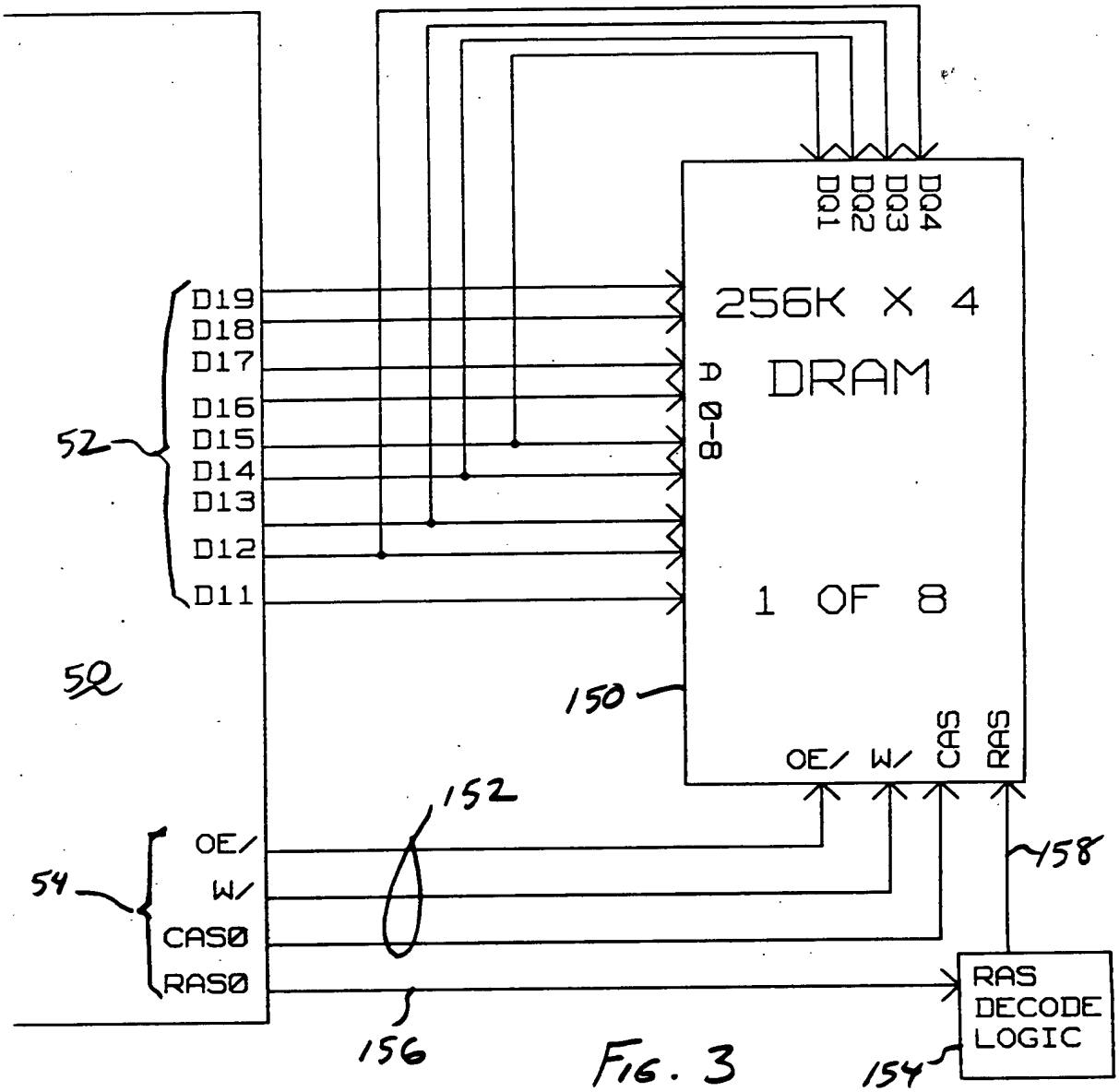


FIG. 3

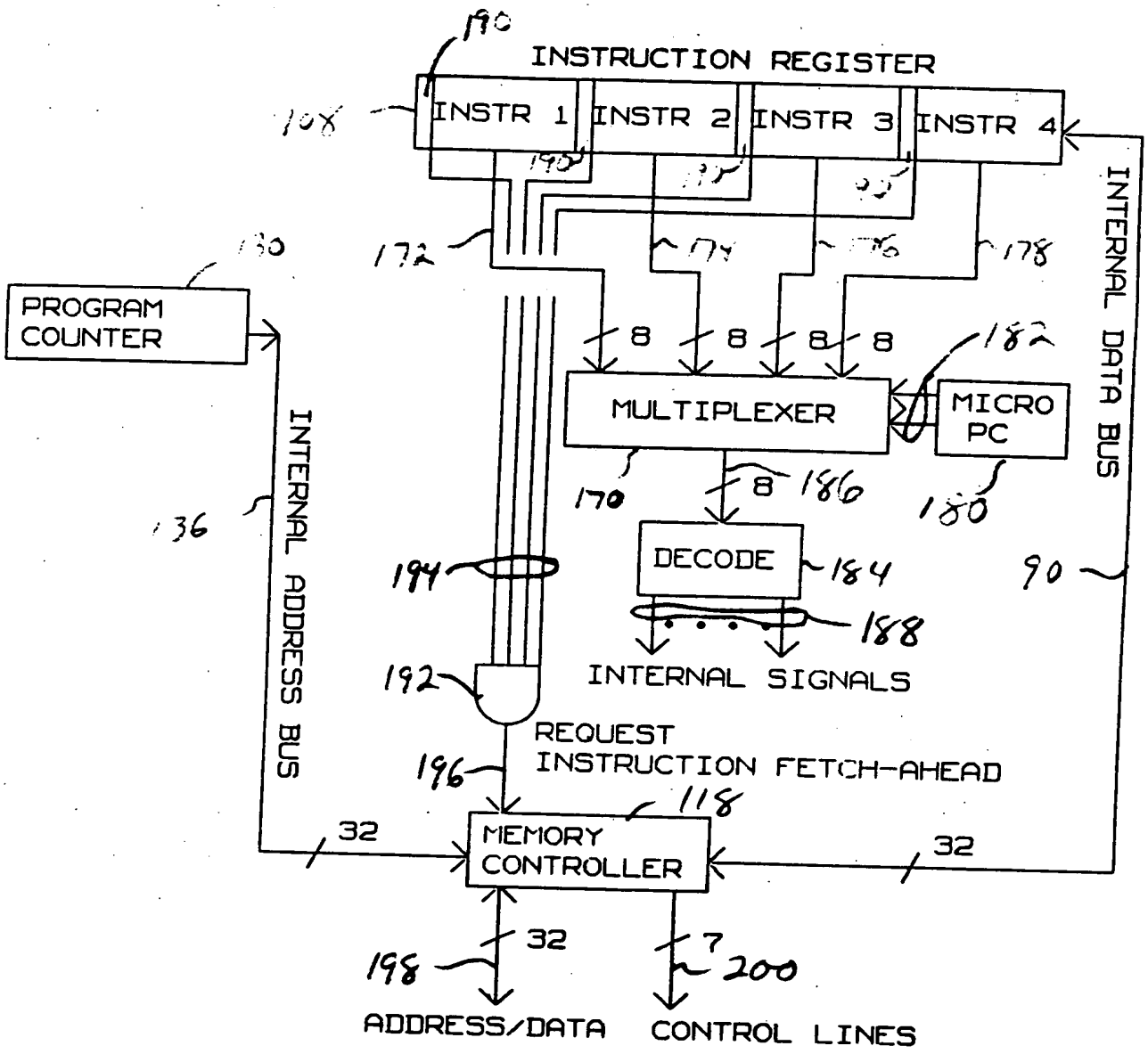
190
INSTRUCTION REGISTER
INSTR 1
INSTR 2
INSTR 3
INSTR 4
INTERNAL DATA BUS
PROGRAM COUNTER
8
8
8
8
MULTIPLEXER
MICRO PC
182
170
8
186
180
DECODE
184
90
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
136
194
192
REQUEST INSTRUCTION FETCH-AHEAD
196
118
32
MEMORY CONTROLLER
32
32
198
7
200
ADDRESS/DATA
CONTROL LINES

Fig. 4

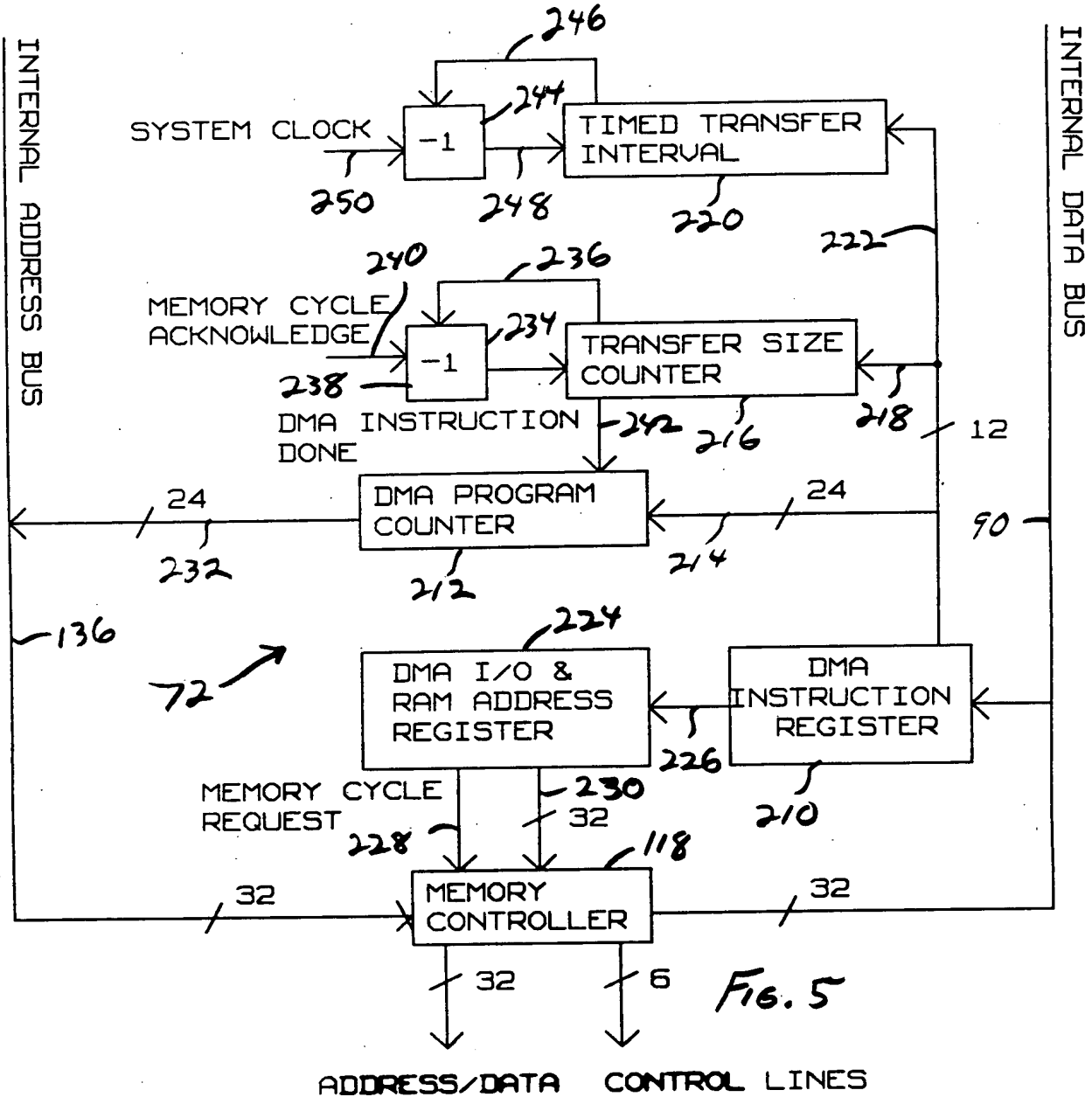
INTERNAL ADDRESS BUS
INTERNAL DATA BUS
SYSTEM CLOCK
-1
TIMED TRANSFER INTERVAL
MEMORY CYCLE ACKNOWLEDGE
-1
TRANSFER SIZE COUNTER
DMA INSTRUCTION DONE
DMA PROGRAM COUNTER
DMA I/O & RAM ADDRESS REGISTER
DMA INSTRUCTION REGISTER
MEMORY CYCLE REQUEST
MEMORY CONTROLLER
ADDRESS/DATA
CONTROL LINES
246
244
250
248
220
222
240
236
234
238
242
216
218
12
24
232
212
24
214
90
136
72
224
226
210
230
32
228
118
32
32
32
6

FIG. 5

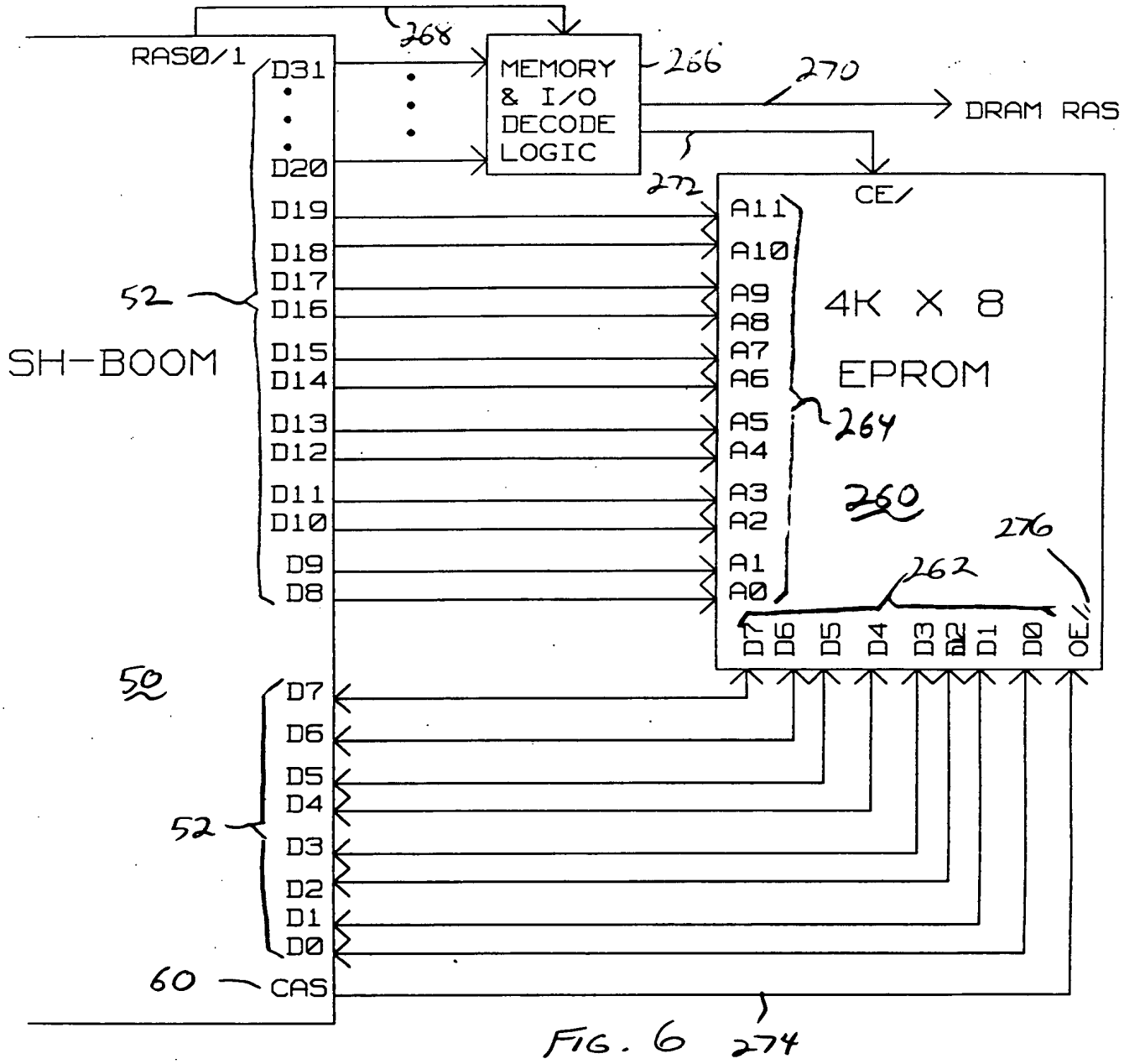
RAS0/1
D31
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
SH-BOOM
268
MEMORY
& I/O
DECODE
LOGIC
266
270
DRAM RAS
272
CE/
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
4K X 8
EPROM
264
260
276
262
D7
D6
D5
D4
D3
D2
D1
D0
OE/
50
52
60
CAS
274

FIG. 6

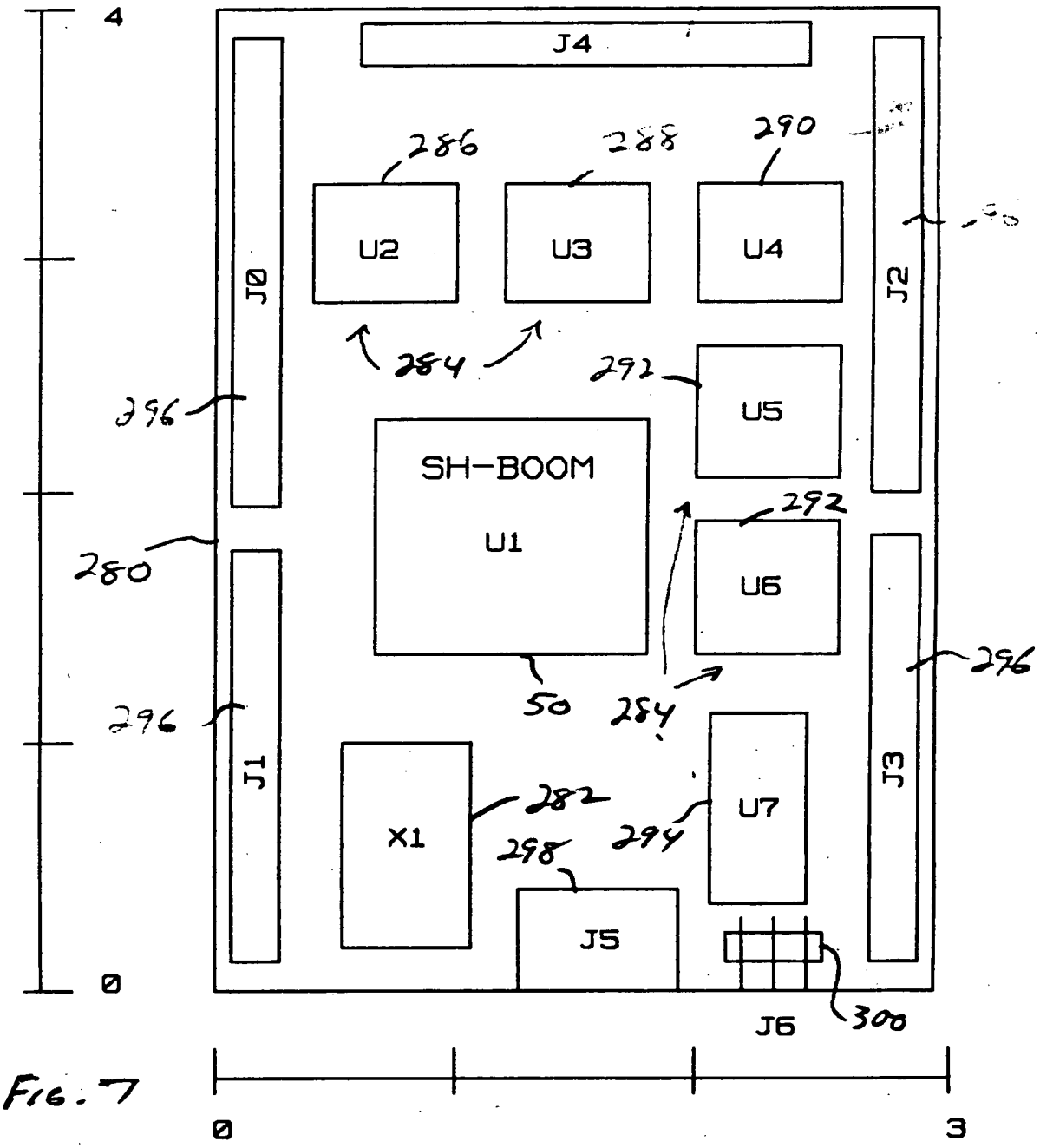
4
0
0
3
J4
J0
J1
J2
J3
J5
J6
U1
SH-BOOM
U2
U3
U4
U5
U6
U7
X1
286
288
290
284
292
296
280
282
294
298
300
50

FIG. 7

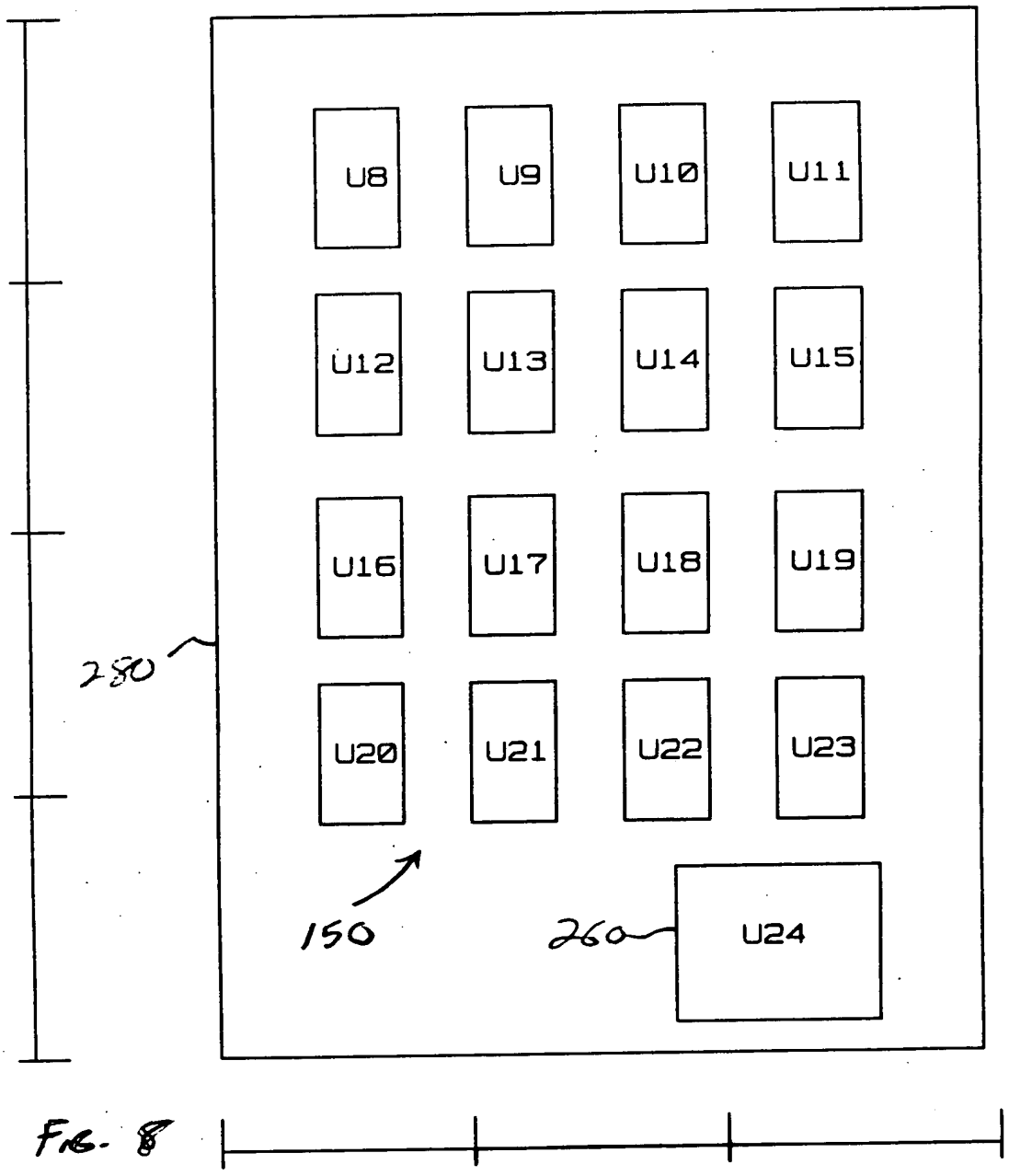
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
280
150
260

FIG. 8

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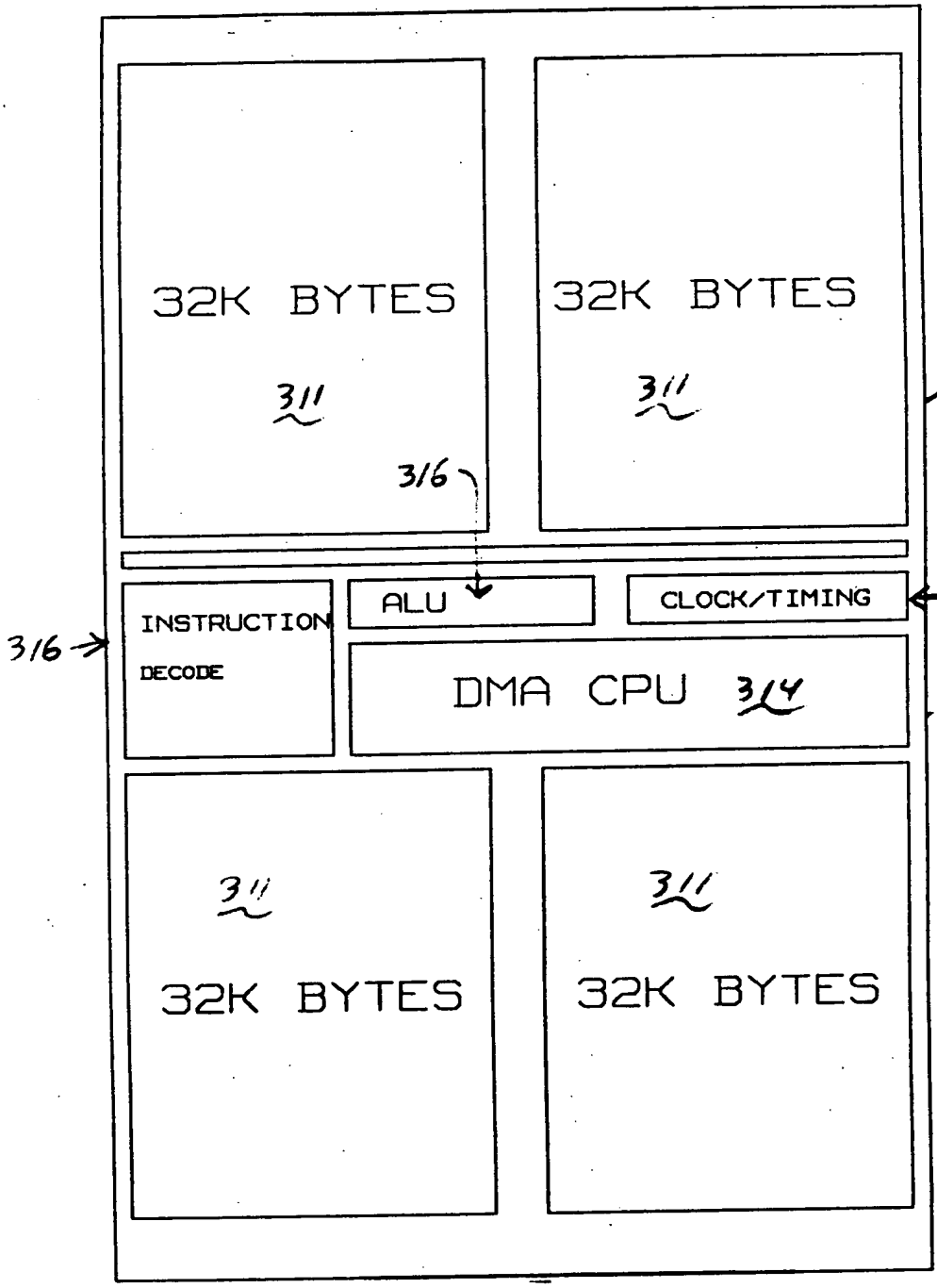
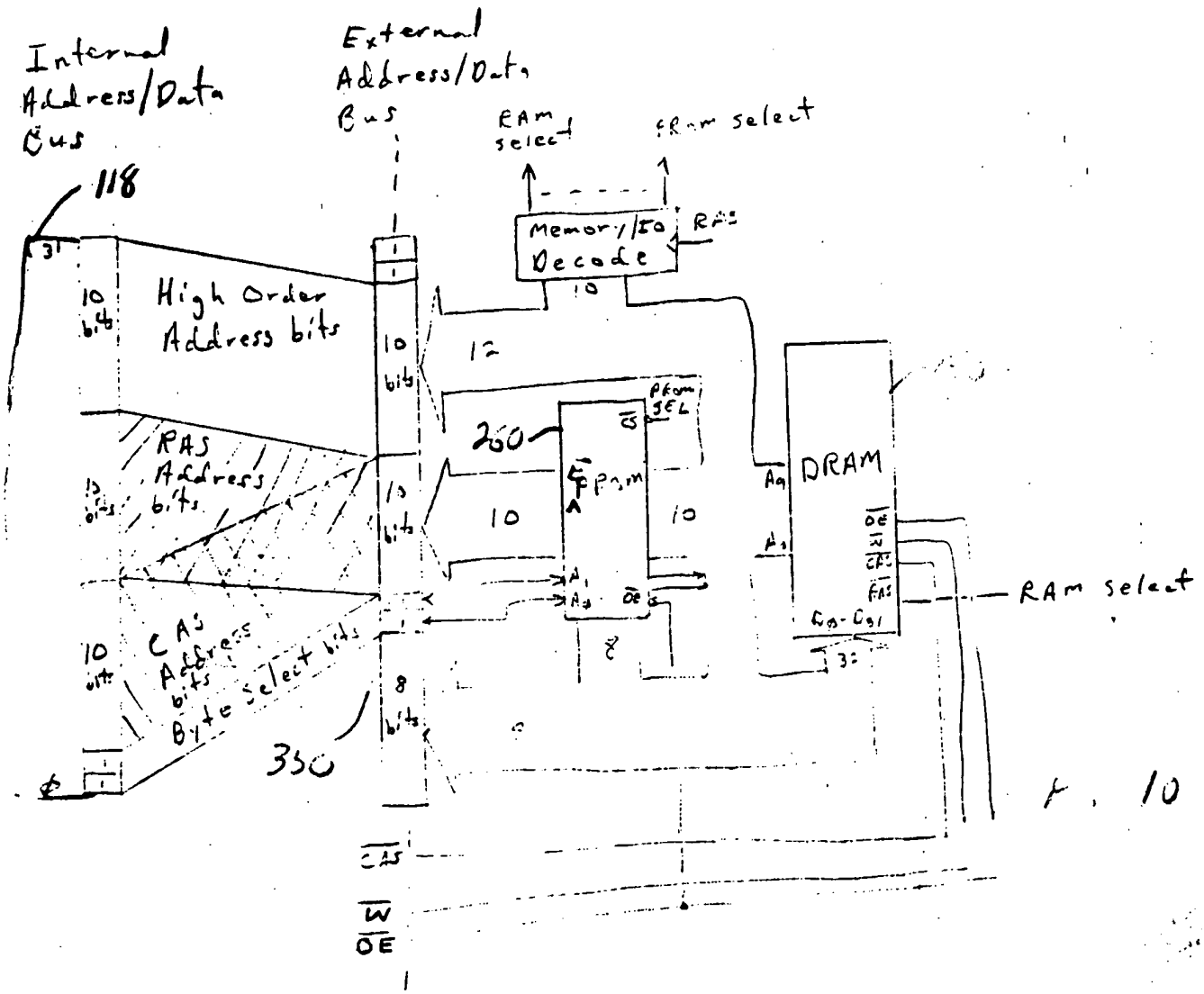



FIG. 9


Internal Address/Data Bus
External Address/Data Bus
118
RAm select
fRam select
Memory/IO Decode
RAS
High Order Address bits
10 bits
12
260
fRam SEL
fRam
DRAM
RAS Address bits
CAS Address bits
Byte select bits
350
RAm select
CAS
W
OE
f. 10

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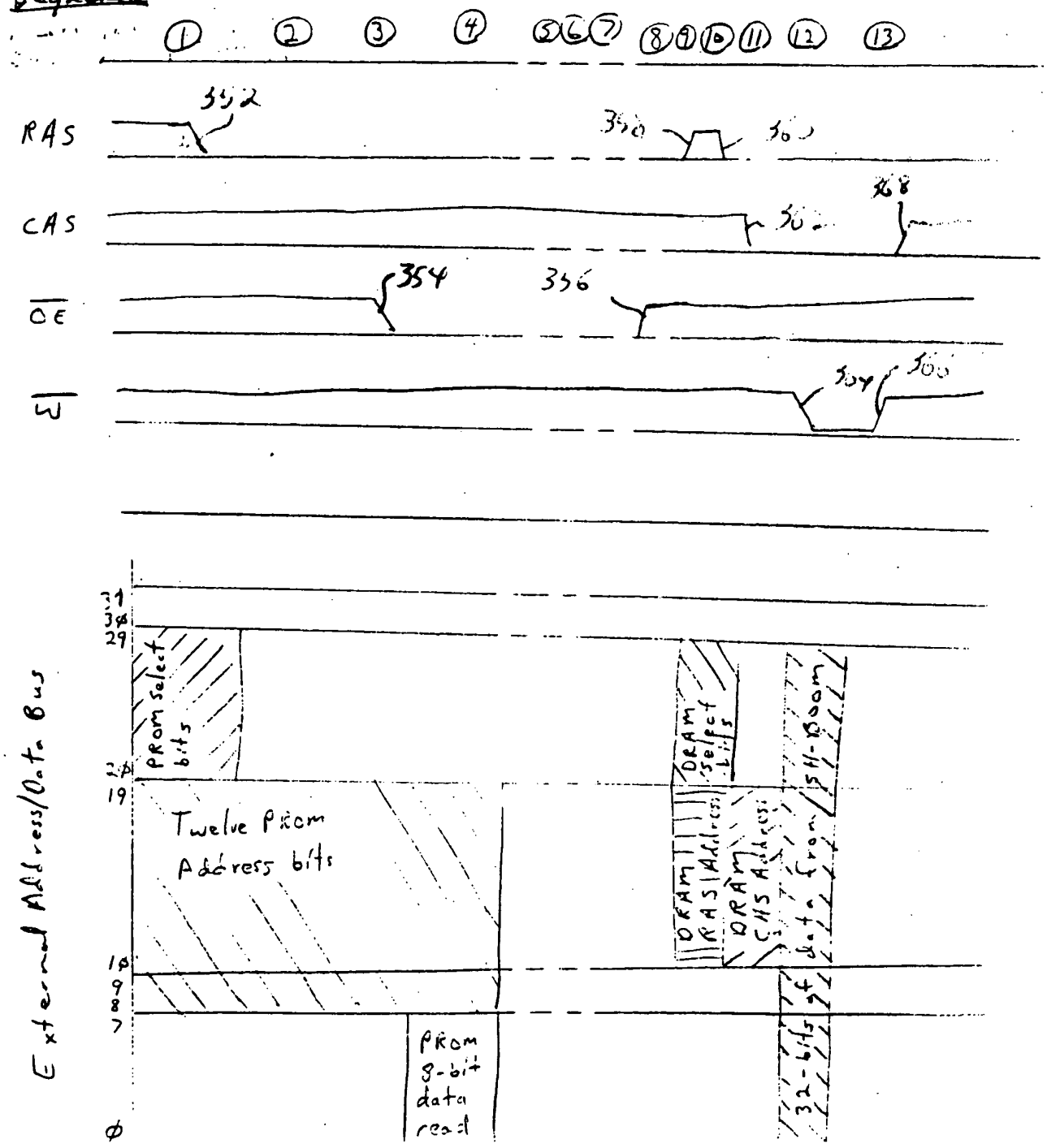


FIG. 11

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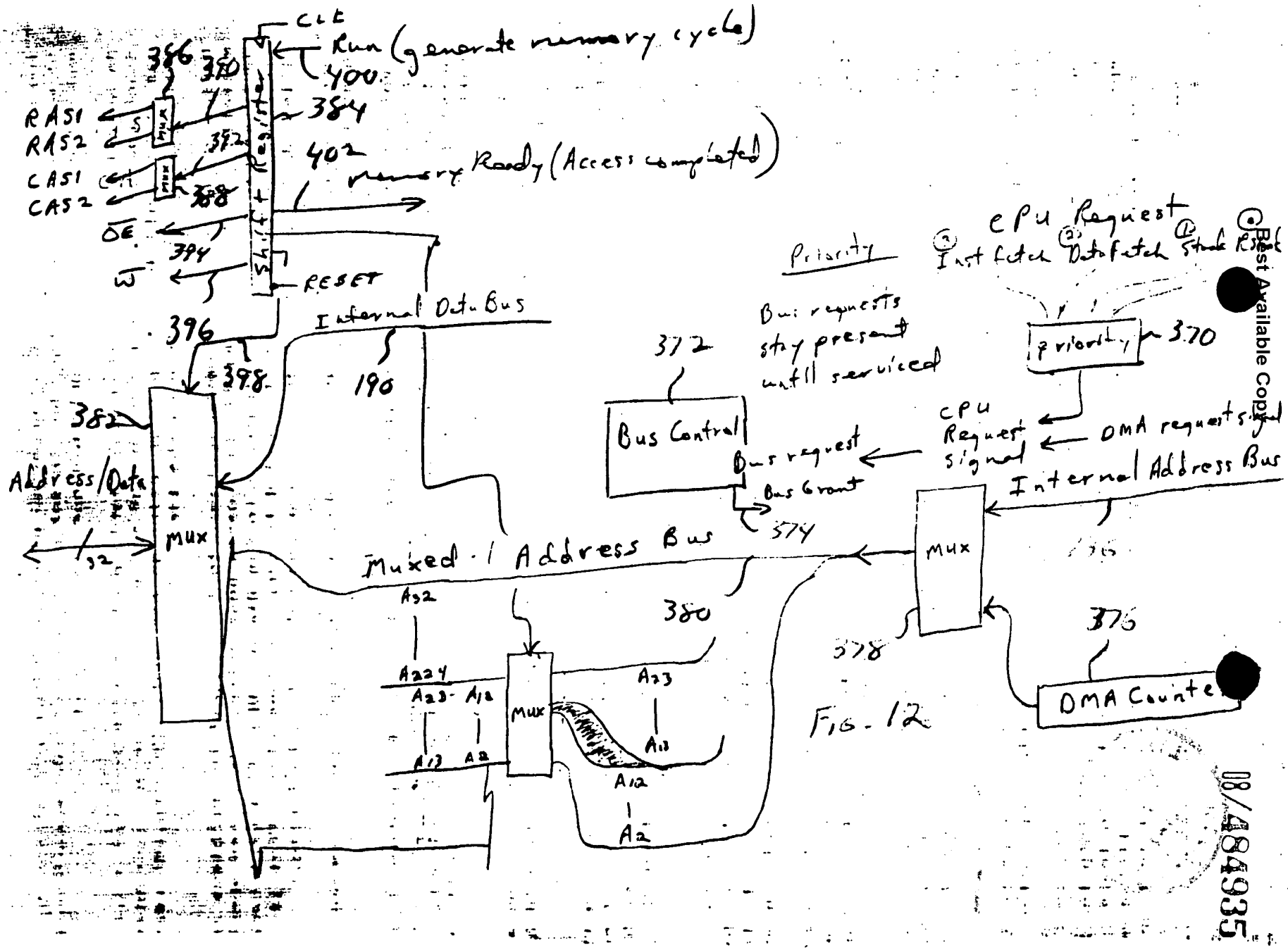
CLK
Run (generate memory cycle)
400
386
320
384
RAS1
RAS2
CAS1
CAS2
382
388
OE
394
W
RESET
402
memory Ready (Access completed)
396
398
Internal Data Bus
190
372
Bus Control
Bus request
Bus Grant
374
Priority
Bus requests stay present until serviced
CPU Request
① Inst fetch ② Data fetch ③ Stack R/W
priority
370
CPU Request signal
DMA request signal
Internal Address Bus
382
Address/Data
32
MUX
Muxed-I Address Bus
380
A32
A24
A23
A13
A12
A2
MUX
MUX
378
376
DMA Counter
FIG. 12
08/484935
Best Available Copy

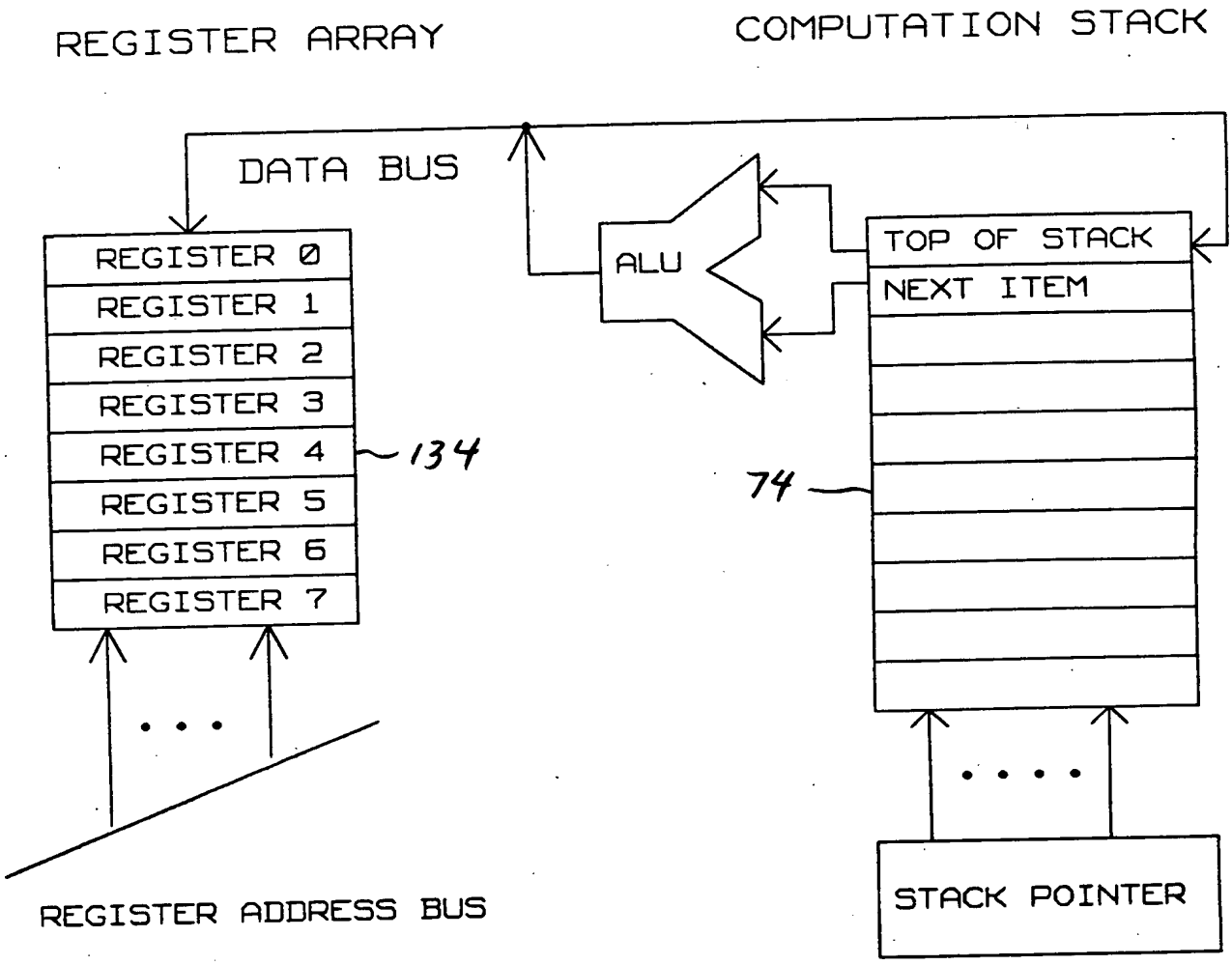
REGISTER ARRAY
COMPUTATION STACK
DATA BUS
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
ALU
TOP OF STACK
NEXT ITEM
74
STACK POINTER
REGISTER ADDRESS BUS

FIG. 13

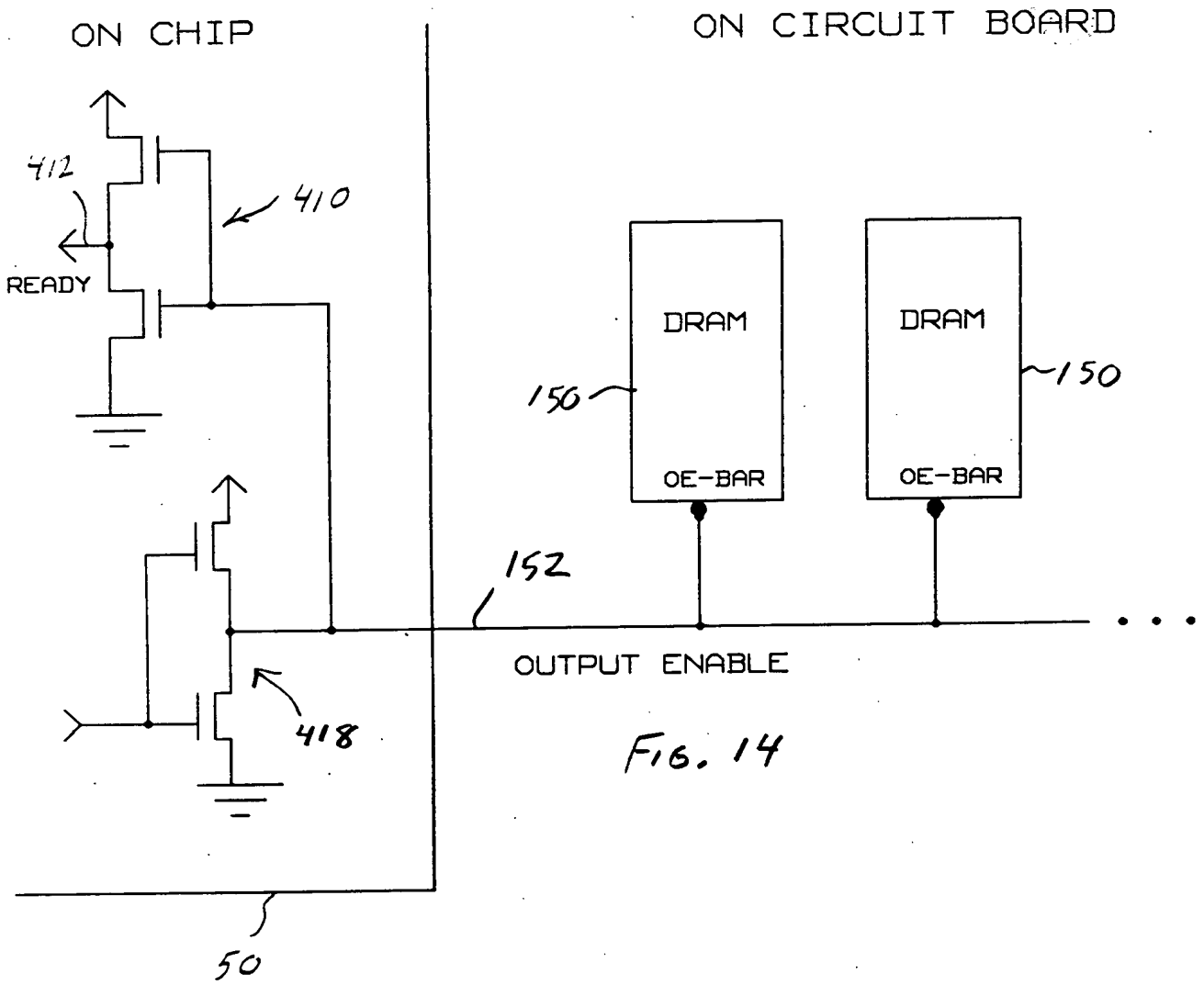
ON CHIP
ON CIRCUIT BOARD
412
410
READY
DRAM
DRAM
150
150
OE-BAR
OE-BAR
152
OUTPUT ENABLE
418
50

FIG. 14

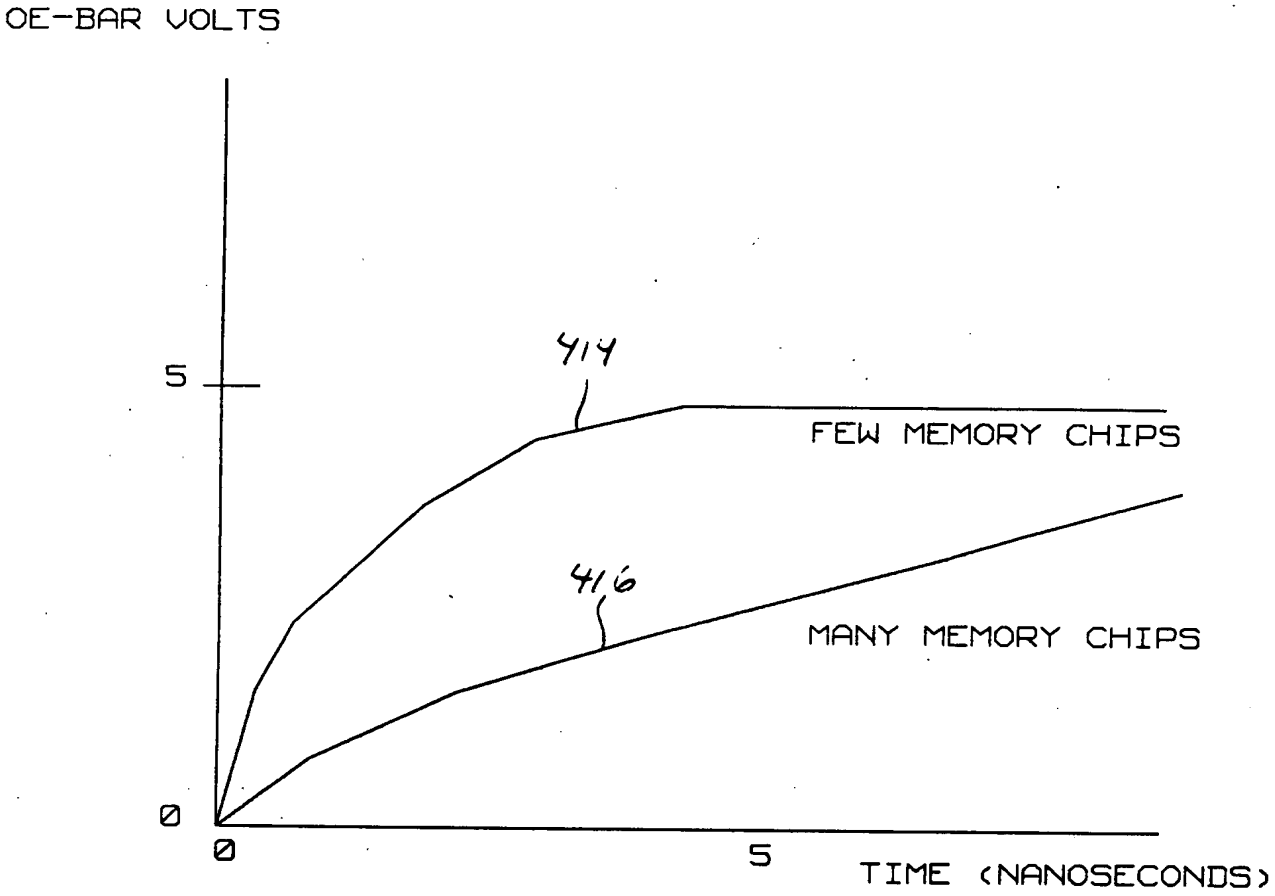
OE-BAR VOLTS
5
0
0
5
414
416
FEW MEMORY CHIPS
MANY MEMORY CHIPS
TIME (NANOSECONDS)

Fig. 15

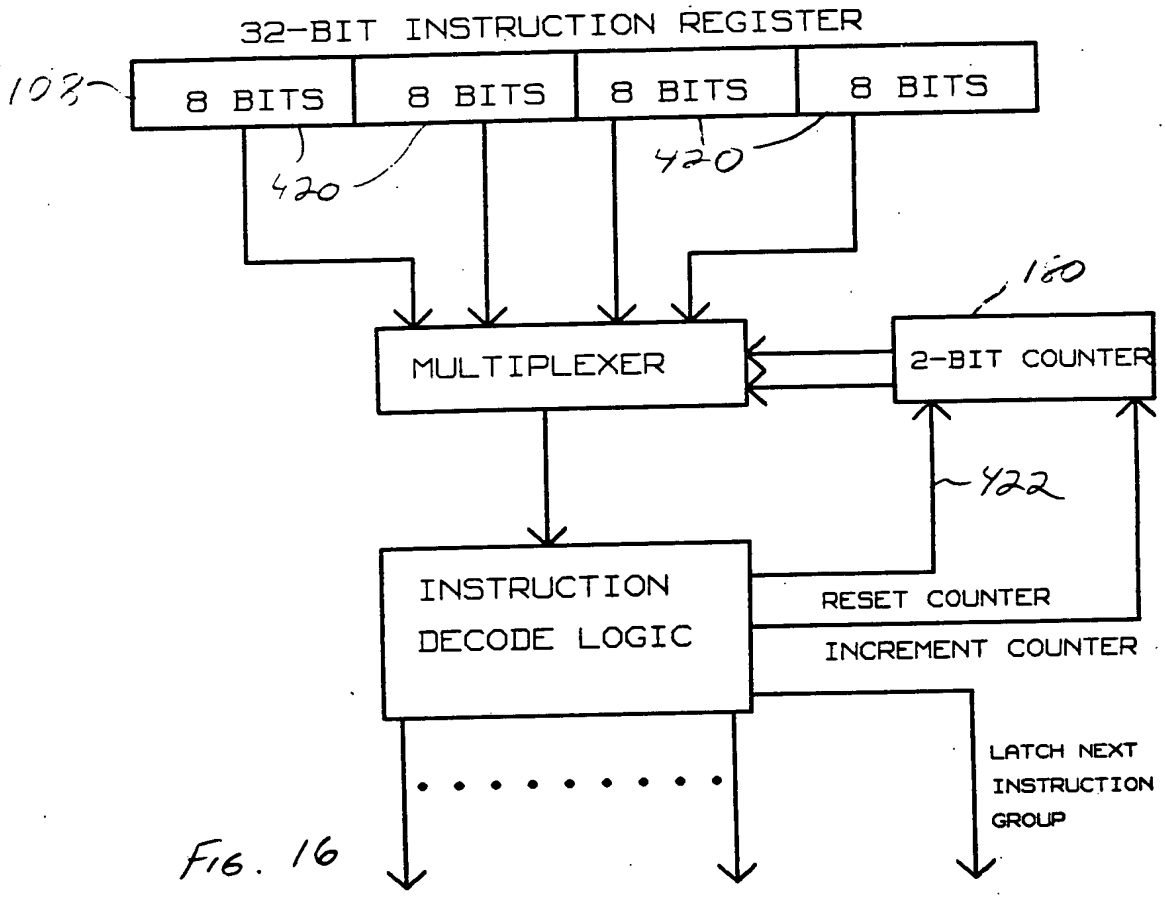
32-BIT INSTRUCTION REGISTER
108
8 BITS
8 BITS
8 BITS
8 BITS
420
420
160
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION
DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT
INSTRUCTION
GROUP
CONTROL SIGNALS

Fig. 16

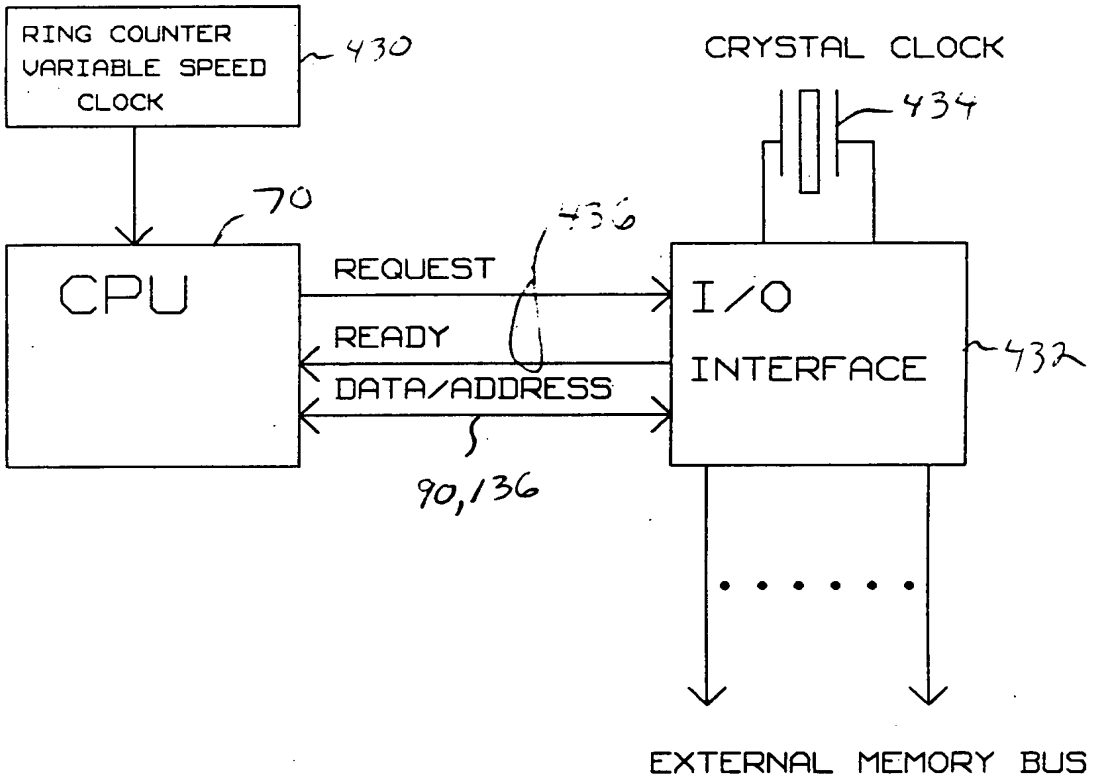
RING COUNTER
VARIABLE SPEED
CLOCK
430
CRYSTAL CLOCK
434
70
436
CPU
REQUEST
READY
DATA/ADDRESS
I/O
INTERFACE
432
90,136
EXTERNAL MEMORY BUS

FIG. 17

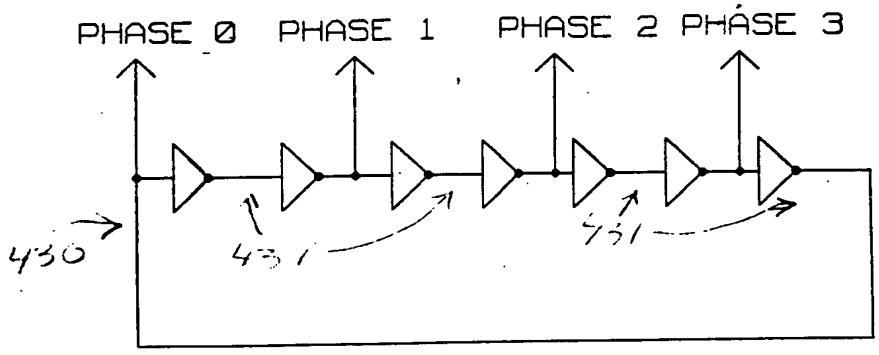
PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG. 18

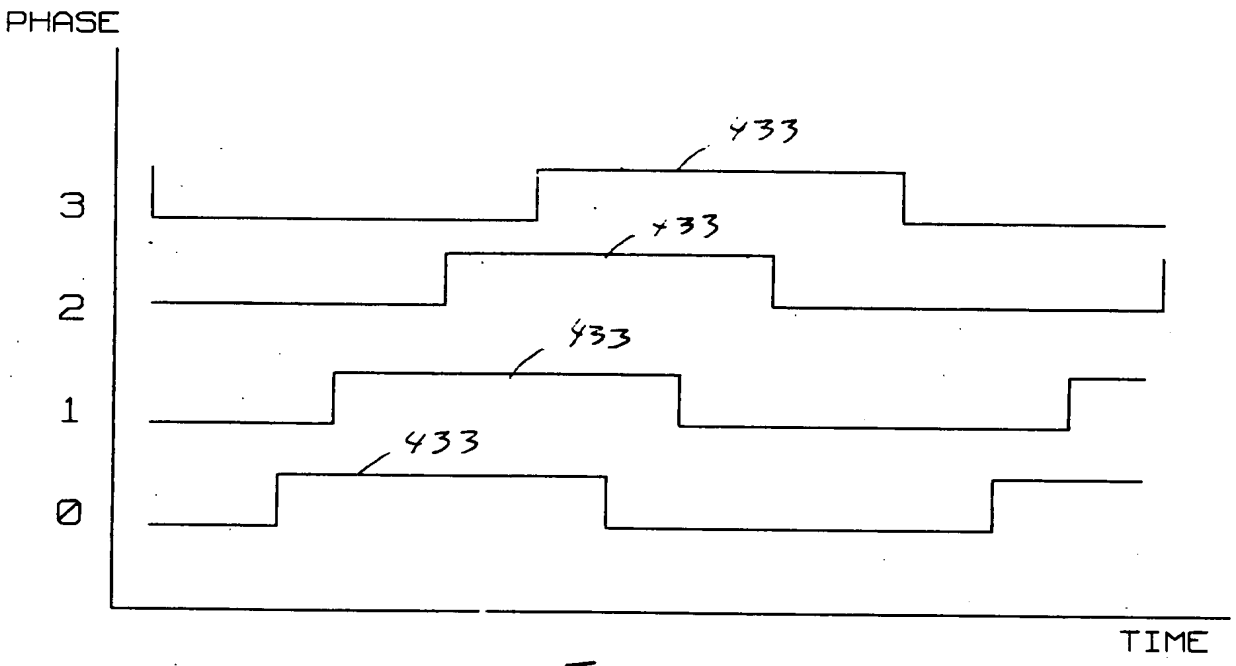
PHASE
3
2
1
0
433
433
433
433
TIME

FIG. 19

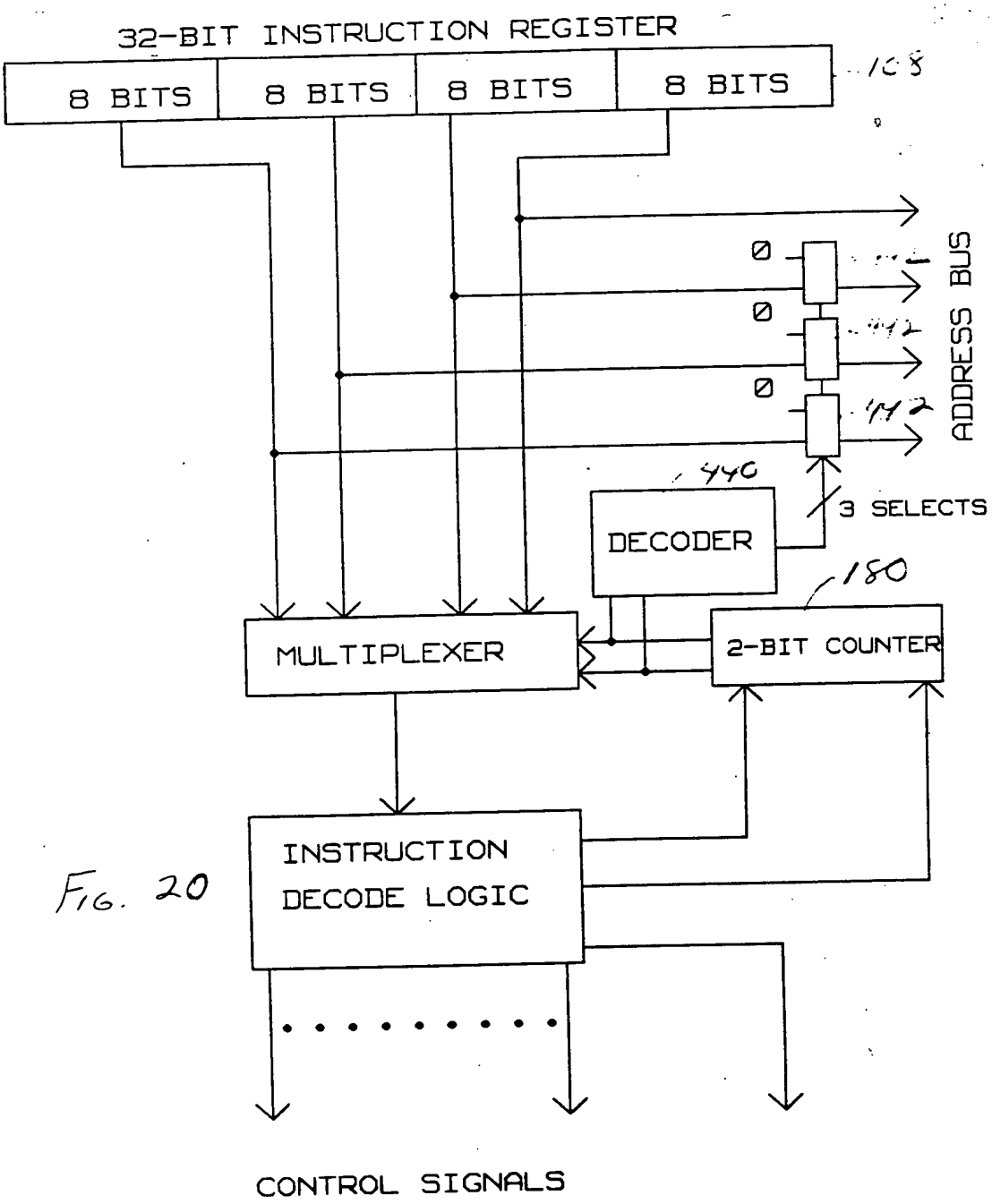
32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
0
0
ADDRESS BUS
440
DECODER
3 SELECTS
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION
DECODE LOGIC
CONTROL SIGNALS

FIG. 20

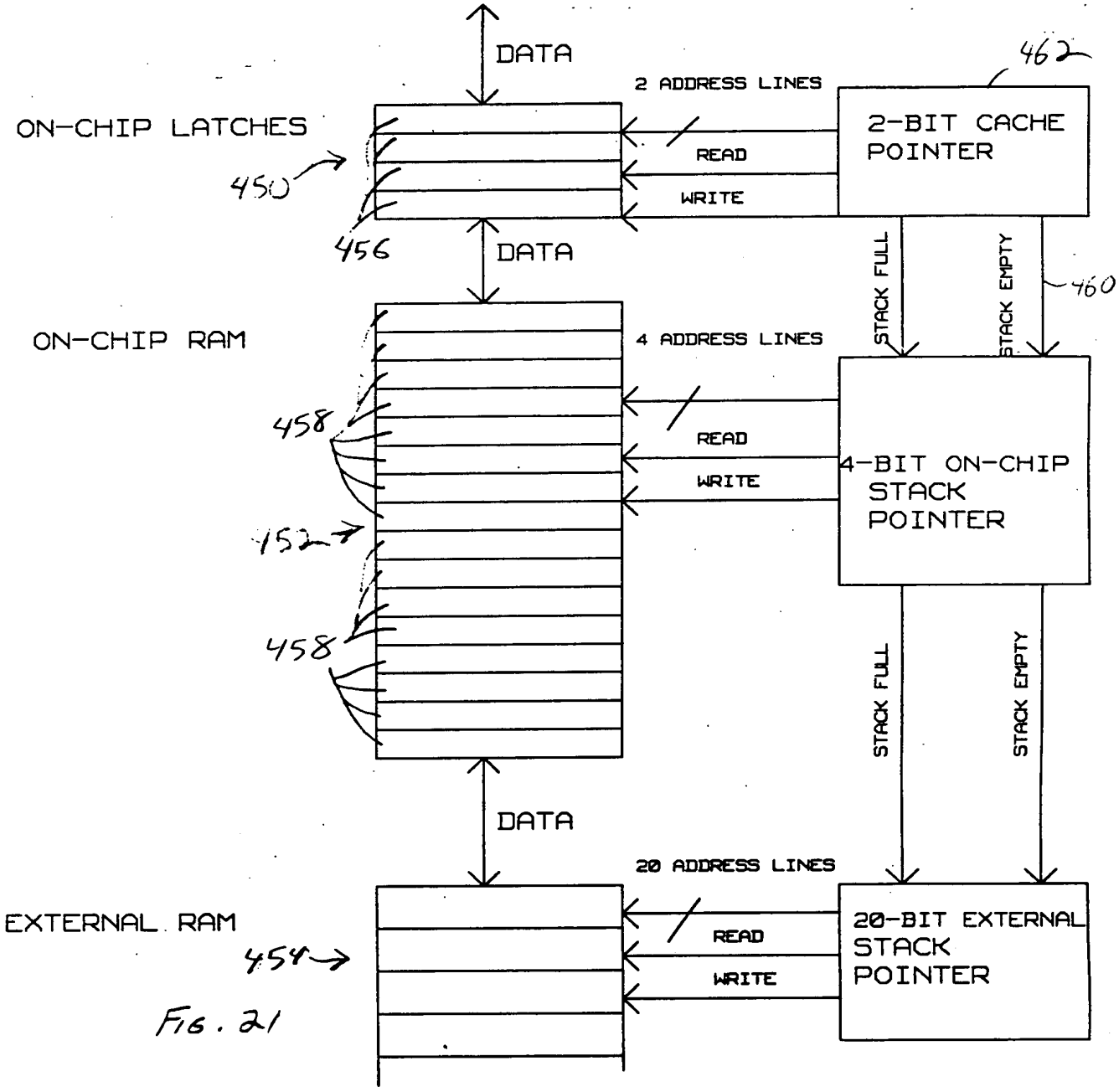
DATA
462
2 ADDRESS LINES
ON-CHIP LATCHES
2-BIT CACHE POINTER
READ
WRITE
450
456
DATA
STACK FULL
STACK EMPTY
460
ON-CHIP RAM
4 ADDRESS LINES
458
READ
4-BIT ON-CHIP STACK POINTER
WRITE
452
458
STACK FULL
STACK EMPTY
DATA
20 ADDRESS LINES
EXTERNAL RAM
READ
20-BIT EXTERNAL STACK POINTER
454
WRITE

Fig. 21

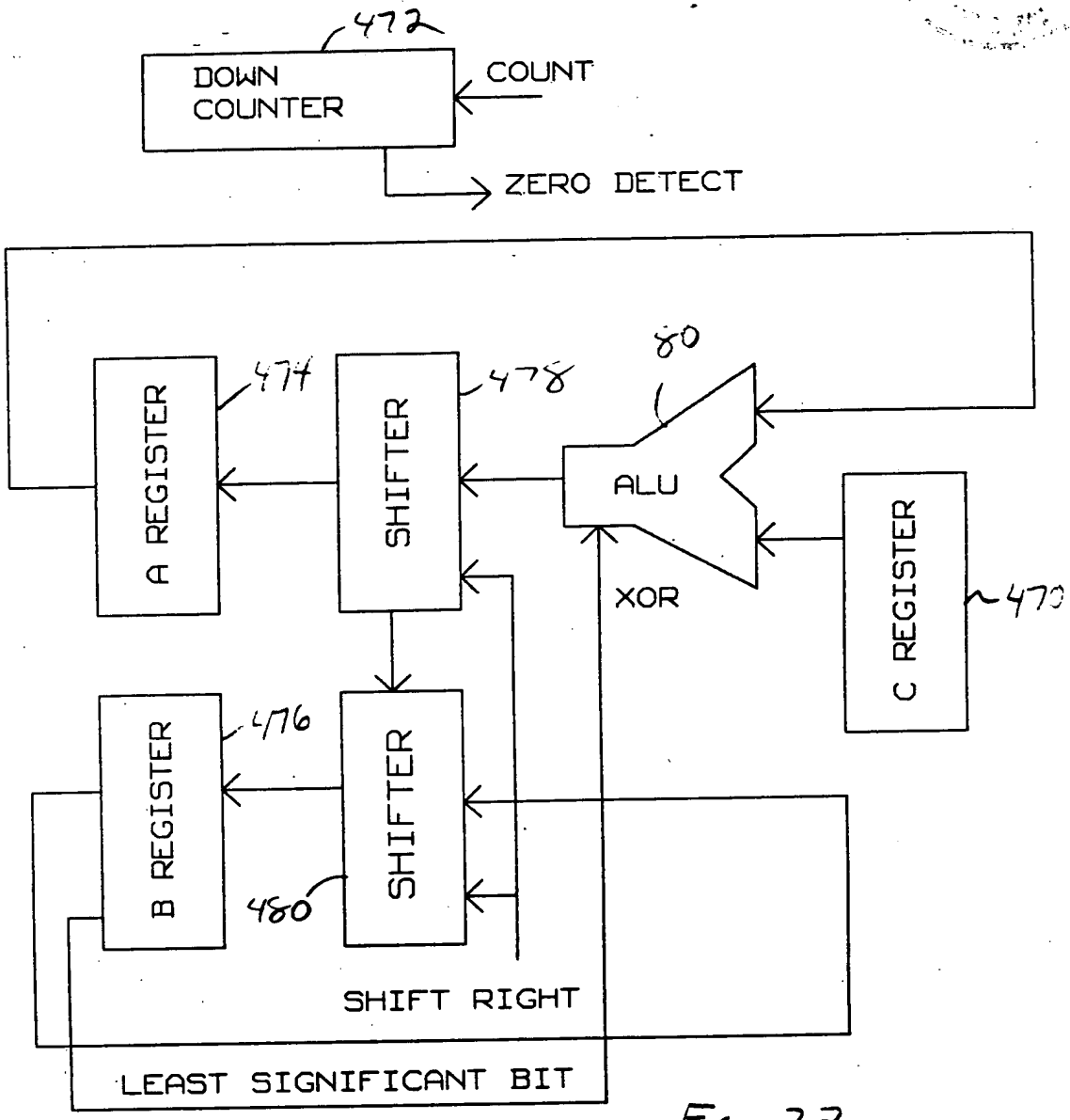
472
DOWN COUNTER
COUNT
ZERO DETECT
80
474
478
A REGISTER
SHIFTER
ALU
XOR
C REGISTER
470
476
B REGISTER
SHIFTER
480
SHIFT RIGHT
LEAST SIGNIFICANT BIT

Fig. 22

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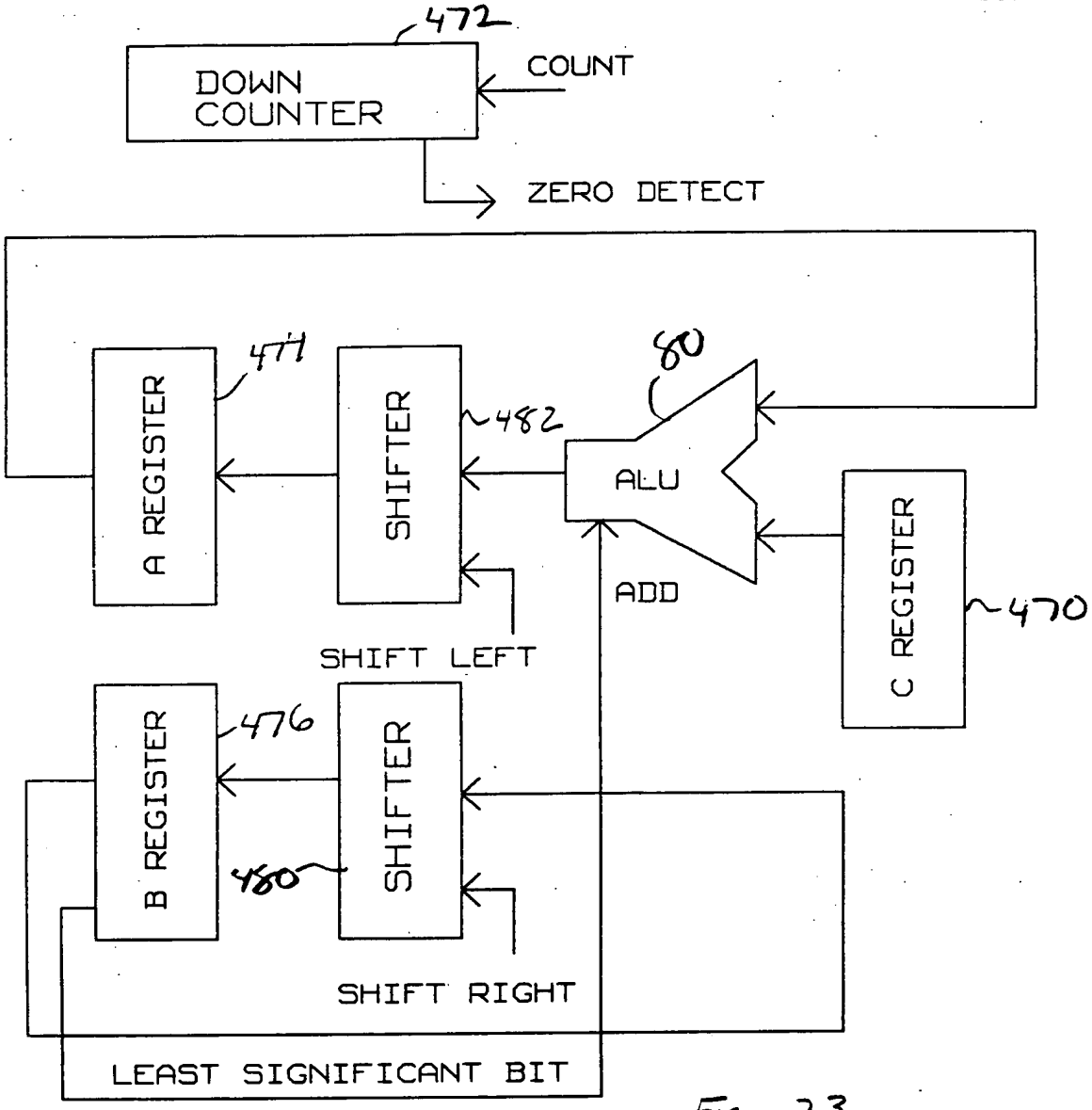


FIG. 23